JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

"AREA AND LATENCY OPTIMIZED EFFICIENT DIGITAL DESIGN OF 32 - BIT RISC PROCESSOR"

A Project report submitted to

Jawaharlal Nehru Technological University Kakinada

in partial fulfillment for the award of the degree of

MASTER OF TECHNOLOGY

In

VLSI AND EMBEDDED SYSTEMS

Submitted by

S.LAKSHMI DEEPIKA

(21H71D6801)

Under the Esteemed Guidance of

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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2022-2023

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CERTIFICATE

This is to certify that the project entitled **"AREA AND LATENCY OPTIMIZED EFFICIENT DIGITAL DESIGN OF 32 - BIT RISC PROCESSOR"** is a bonafide work carried out by **Lakshmi Deepika. S (21H71D6801)**, in partial fulfillment for the award of degree of master of Technology in **VLSI & EMBEDDED SYSTEMS** of **DVR & Dr. HS MIC College of Technology** during the year **2022-2023.**

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Examiner I

Examiner II

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

"HARDWARE IMPLEMENTATION OF AES IN FPGA"

A Project report submitted to
Jawaharlal Nehru Technological University Kakinada
In partial fulfillment for the award of degree of

MASTER OF TECHNOLOGY

IN

VLSI AND EMBEDDED SYSTEMS

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This is to certify that the project entitled **"HARDWARE IMPLEMENTATION OF AES IN FPGA"** is a bonafide work carried out by **Nathan. P (21H71D6802)**, in partial fulfillment for the award of the degree of master of technology in **VLSI & EMBEDDED SYSTEMS of DVR & Dr. HS MIC College of Technology during the year 2022-2023.**

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