ACADEMIC REGULATIONS

(MIC18)

COURSE STRUCTURE

&

SYLLABUS

For

MASTER OF TECHNOLOGY

(M.Tech)

ECE/VLSI & EMBEDDED SYSTEMS

(Applicable for batches admitted from 2018-19 onwards)

Devineni Venkata Ramana & Dr. Himasekhar

MIC College of Technology

An Autonomous Institution

Approved by AICTE, Permanently Affiliated to: JNTUK, Kakinada

Kanchikacherla - 521180, Krishna Dist, A.P, India.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
PROPOSED COURSE STRUCTURE (Autonomous)
for M.Tech (VLSI and Embedded Systems)
I Year I Semester

Sr. No.	Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
1	18411T01	Digital System Design	3	0	0	3	3
2	18411T02	Embedded Real Time Operating Systems	3	0	0	3	3
3	18411T03 18411T04 18411T05	**Programme Elective I** 1. VLSI Technology and Design 2.CMOS Digital IC Design 3. System on Chip Design	3	0	0	3	3
4	18411T06 18411T07 18411T08	**Programme Elective II** 1. Advanced Operating Systems 2. Soft Computing Techniques 3. Network Security and Cryptography	3	0	0	3	3
5	18411L09	VLSI System design Lab-I	0	0	4	2	2
6	18411L10	Digital System Design using Verilog and VHDL	0	0	4	2	2
7	18411T11	Research Methodology	2	0	0	2	2
						Total Credits	**18**

I Year II Semester

Sr. No.	Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
1	18412T01	Embedded system Design	3	0	0	3	3
2	18412T02	Low Power VLSI Design	3	0	0	3	3
3	18412T03 18412T04 18412T05	**Programme Elective III** 1. VLSI Signal Processing 2. CMOS Mixed Signal Circuit Design 3. CPLD & FPGA Architectures and Applications.	3	0	0	3	3
4	18412T06 18412T07 18412T08	**Programme Elective IV** 1.Micro Electro Mechanical Systems (MEMS) Design 2. DSP Processors & Architectures 3. Semiconductor Memory Design and Testing.	3	0	0	3	3
5	18412L09	Embedded System Design lab	0	0	4	4	2
6	18412L10	VLSI System design Lab-II	0	0	4	4	2
7	18412T11	Intellectual Property Rights And Patents	2	0	0	2	2
						Total Credits	**18**

II Year III Semester

Sr. No.	Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
1	18413T01 18413T02 18413T03	**Programme Elective V** 1. Advanced Computer Architecture 2. ASIC Design 3. Design for IOT	3	0	0	3	3
2	18413T04 18413T05 18413T06	**Programme Elective VI** 1. Image and Video Processing 2. Wireless communications and Networks 3. Multimedia Systems	3	0	0	3	3
3	18413P07	Project Work part-1	0	0	20	20	10
						Total Credits	**16**

II Year IV Semester

Sr. No.	Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
1	18414S01	Comprehensive Viva-Voce	0	0	4	4	2
2	18414P02	Project Work Part -II	0	0	28	28	14
						Total Credits	**16**

Dr.M Rama Subba Reddy

Dr. Anil Kumar

Dr.I Santhi Prabha

Mr.N Pradeep

18/6/18

Dr. Goutam Kumar Gupta

I-Year I Semester

Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18411T01	Digital System Design	3	0	0	3	3

UNIT-I

Minimization Procedures and CAMP Algorithm

Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs,, CAMP-I algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

UNIT-II

PLA Design, PLA Minimization and Folding Algorithms

Introduction to PLDs, basic configurations and advantages of PLDs, PLA Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm(IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.

UNIT –III

Design of Large Scale Digital Systems

Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT-IV

Fault Diagnosis in Combinational Circuits

Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.

UNIT-V

Fault Diagnosis in Sequential Circuits

Fault detection and location in sequential circuits, circuit test approach, initial state identification, Haming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

TEXT BOOKS:

1. Logic Design Theory-N. N. Biswas, PHI
2. Switching and Finite Automata Theory-Z. Kohavi , 2nd Edition, 2001,TMH
3. Digital system Design using PLDd-Lala

REFERENCE BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.

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MIC College of Technology

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Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18411T02	Embedded Real Time Operating Systems	3	0	0	3	3

UNIT-I

Introduction

Introduction to Operating Systems Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT-II

RTOS Introduction

OS Services, Process Management, Timer Functions, Event Functions, Memory Management, Device, File and IO Systems Management, Interrupt Routines in RTOS Environment and Handling of Interrupt Source Calls, Real-Time Operating Systems, Basic Design Using an RTOS, RTOS Task Scheduling Models, Interrupt Latency and Response of the Tasks as Performance Metrics, OS Security Issues.

UNIT-III

RTOS Programming

Basic Functions and Types of RTOS for Embedded Systems, RTOS mCOS-II, RTOS Vx Works, Programming concepts of above RTOS with relevant Examples, Programming concepts of RTOS Windows CE, RTOS OSEK, RTOS Linux 2.6.x and RTOS RT Linux.

UNIT-IV

Program Modeling – Case Studies

Case study of embedded system design and coding for an Automatic Chocolate Vending Machine (ACVM) Using Mucos RTOS, case study of digital camera hardware and software architecture, case study of coding for sending application layer byte streams on a TCP/IP Network Using RTOS Vx Works, Case Study of Embedded System for an Adaptive Cruise Control (ACC) System in Car, Case Study of Embedded System for a Smart Card, Case Study of Embedded System of Mobile Phone Software for Key Inputs.

UNIT-V

Target Image Creation & Programming in Linux

Off-The-Shelf Operating Systems, Operating System Software, Target Image Creation for Window XP Embedded, Porting RTOS on a Micro Controller based Development Board. Overview and programming concepts of Unix/Linux Programming, Shell Programming and System Programming.

TEXT BOOKS:

1. Dr. K.V.K.K. Prasad: "Embedded/Real-Time Systems" Dream Tech Publications, Black pad book.
2. Rajkamal: "Embedded Systems-Architecture, Programming and Design", Tata McGraw Hill Publications, Second Edition, 2008.

REFERENCES:

1. Rob Williams," Real time Systems Development", Butterworth Heinemann Publications.

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Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18411T03	Programme Elective- I VLSI Technology and Design	3	0	0	3	3

UNIT-I

VLSI Technology

Fundamentals and applications, IC production process, semiconductor processes, design rules and process parameters, layout techniques and process parameters. **VLSI Design Issues**: Design process, design for testability, technology options, power calculations, package selection, clock mechanisms, mixed signal design.

UNIT-II

VLSI Design: Electronic design automation concept, ASIC and FPGA design flows, SOC designs, design technologies: combinational design techniques, sequential design techniques, state machine logic design techniques and design issues.

UNIT-III

CMOS VLSI Design: MOS Technology and fabrication process of pMOS, nMOS, CMOS and BiCMOS technologies, comparison of different processes. **Building Blocks of a VLSI circuit**: Computer rchitecture, memory architectures, communication interfaces, mixed signal interfaces.

UNIT-IV

Basic electrical properties of MOS and BiCMOS circuits, MOS and BiCMOS circuit design processes, Basic circuit concepts, scaling of MOS circuits-qualitatitive and quantitative analysis with proper illustrations and necessary derivations of expressions.

UNIT-V

Subsystem Design and Layout: Some architectural issues, switch logic, gate logic, examples of structured design (combinational logic), some clocked sequential circuits, other system considerations. **Subsystem Design Processes:** Some general considerations and an illustration of design processes, design of an ALU subsystem. Floor Planning

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A. Pucknell, Sholeh Eshraghian, 2005, PHI Publications.
2. Modern VLSI Design-Wayne Wolf, 3rd Ed., 1997, Pearson Education.
3. VLSI Design-Dr.K.V.K.K.Prasad, Kattula Shyamala, Kogent Learning Solutions Inc., 2012.

REFERENCE BOOKS:

1. VLSI Design Technologies for Analog and Digital Circuits, Randall L.Geiger, Phillip E.Allen, Noel R.Strader, TMH Publications, 2010.
2. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming-BO Lin, CRC Press, 2011.

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Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18411T04	Programme Elective- I CMOS Digital IC Design	3	0	0	3	3

UNIT-I

MOS Devices and Modeling The MOS Transistor, Passive Components-Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT-II

MOS Design Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-III

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-IV

Sequential MOS Logic Circuits Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT-V

Dynamic Logic Circuits Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits. Semiconductor Memories

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

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Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18411T05	**Programme Elective- II** **System on Chip Design**	3	0	0	3	3

UNIT-I

Introduction to the System Approach

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT-II

Processors Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT-III

Memory Design for SOC Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT-IV

Interconnect Customization and Configuration Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

UNIT-V

SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

Application Studies / Case Studies SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques – Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

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Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18411T06	**Programme Elective- II** **Advanced Operating Systems**	3	0	0	3	3

UNIT-I

Introduction to Operating Systems Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT-II

Introduction to UNIX and LINUX Basic Commands & Command Arguments, Standard Input, Output, Input / Output Redirection, Filters and Editors, Shells and Operations

UNIT –III

System Calls: System calls and related file structures, Input / Output, Process creation & termination.
Inter Process Communication : Introduction, File and record locking, Client – Server example, Pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV

Introduction to Distributed Systems: Goals of distributed system, Hardware and software concepts, Design issues. **Communication in Distributed Systems:** Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT –V

Synchronization in Distributed Systems: Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions **Deadlocks:** Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.
EMBEDDED OS: Discussions on Basics of Linux supportive RTOS – uCOS-C Executive for development of RTOS Application –introduction to Android Environment -The Stack – Android User Interface – Preferences, the File System, the Options Menu and Intents, with one Case study

TEXT BOOKS:

1. The Design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete Reference LINUX – Richard Peterson, 4th Ed., McGraw –Hill.

REFERENCE BOOKS:

1. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.
2. Modern Operating Systems - Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles - Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley

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Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18411T07	Programme Elective- I Soft Computing Techniques	3	0	0	3	3

UNIT –I

Introduction: Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, and Knowledge representation - Expert systems.

UNIT –II

Artificial Neural Networks: Introduction, Humans and Computers, Organization of the Brain, Biological Neuron, Biological and Artificial Neuron Models, Characteristics of ANN, McCulloch-Pitts Model, Historical Developments, Potential Applications of ANN, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network.

UNIT-III

Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT –IV

Fuzzy Logic System: Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self-organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT –V

Genetic Algorithm: Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search techniques for solving optimization problems, Applications.

TEXT BOOKS:

1. Introduction to Artificial Neural Systems - Jacek.M.Zurada, Jaico Publishing House, 1999.
2. Neural Networks and Fuzzy Systems - Kosko, B., Prentice-Hall of India Pvt. Ltd., 1994.

REFERENCE BOOKS:

1. Fuzzy Sets, Uncertainty and Information - Klir G.J. & Folger T.A., Prentice-Hall of India Pvt. Ltd.,
2. Fuzzy Set Theory and Its Applications - Zimmerman H.J. Kluwer Academic Publishers, 1994.
3. Introduction to Fuzzy Control - Driankov, Hellendroon, Narosa Publishers.
4. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.
5. Elements of Artificial Neural Networks - Kishan Mehrotra, Chelkuri K. Mohan, Sanjay Ranka, Penram International.

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MIC College of Technology

(Autonomous)

Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18411T08	**Programme Elective- II** **Network security and Cryptography**	3	0	0	3	3

UNIT-I

Introduction Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security. Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT-II

Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations. **Algorithms:** Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.

UNIT-III

Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation. Public Key **Cryptography:** Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT-IV

Number Theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms. Message authentication and Hash Functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT-V

Hash and Mac Algorithms: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. Digital signatures and Authentication Protocols: Digital signatures, Authentication Protocols, Digital signature standards. Authentication Applications: Kerberos, X.509 directory Authentication service. Electronic Mail Security: Pretty Good Privacy, S/MIME, IP Security.

TEXT BOOKS:

1. Cryptography and Network Security: Principles and Practice – William Stallings, 2000, PE.

REFERENCE BOOKS:

1. Principles of Network and Systems Administration, Mark Burgess,John Wiey.

G. A. Lakshmi

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Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18411T09	Research Methodolgy	2	0	0	2	2

Unit-I

Foundations of Research: Meaning, Objectives, Motivation, Utility. Concept of theory, empiricism, deductive and inductive theory. Characteristics of scientific method – Understanding the language of research – Concept, Construct, Definition, Variable. Research Process. Problem Identification & Formulation – Research Question – Investigation Question – Measurement Issues – Hypothesis – Qualities of a good Hypothesis –Null Hypothesis & Alternative Hypothesis. Hypothesis Testing – Logic & Importance

Unit-II

Research Design: Concept and Importance in Research – Features of a good research design – Exploratory Research Design – concept, types and uses, Descriptive Research Designs – concept, types and uses. Experimental Design: Concept of Independent & Dependent variables.

UNIT-III

Qualitative and Quantitative Research: Qualitative research – Quantitative research – Concept of measurement, causality, generalization, replication. Merging the two approaches. Concept of measurement– what is measured? Problems in measurement in research – Validity and Reliability. Levels of measurement – Nominal, Ordinal, Interval, Ratio.

UNIT-IV

Sampling: Concepts of Statistical Population, Sample, Sampling Frame, Sampling Error, Sample Size, Non Response. Characteristics of a good sample. Probability Sample – Simple Random Sample, Systematic Sample, Stratified Random Sample & Multi-stage sampling. Determining size of the sample – Practical considerations in sampling and sample size.

Unit-V

Data Analysis: Data Preparation – Univariate analysis (frequency tables, bar charts, pie charts, percentages), Bivariate analysis – Cross tabulations and Chi-square test including testing hypothesis of association. Interpretation of Data and Paper Writing – Layout of a Research Paper, Journals in Computer Science, Impact factor of Journals, When and where to publish ? Ethical issues related to publishing, Plagiarism and Self-Plagiarism, Use of Encyclopedias and Tools.

Text Books:-

1. Business Research Methods – Donald Cooper & Pamela Schindler, TMGH, 9th edition
2. Business Research Methods – Alan Bryman & Emma Bell, Oxford University Press.
3. Research Methodology – C.R.Kothari

G. A. Lakshmi
M. Gopala Krishna
(K. Thirupathi Rao)

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MIC College of Technology

(Autonomous)

Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18411L10	VLSI System design Lab-I	0	0	4	2	2

PART-A: VLSI Lab (Front-end Environment)

• The students are required to design the logic circuit to perform the following experiments using necessary simulator to verify the logical / functional operation and to perform the analysis with appropriate synthesizer (Mentor Graphics Precision RTL) and then verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).

• The students are required to acquire the knowledge in the Platforms (Mentor graphics) by perform at least SIX experiments on each Platform.

List of Experiments:

1. Realization of Logic gates.
2. Parity Encoder.
3. Random Counter
4. Synchronous RAM.
5. ALU.
6. UART Model.
7. Fire Detection and Control System using Combinational Logic circuits.
8. Traffic Light Controller using Sequential Logic circuits
9. Pattern Detection using Moore Machine.
10. Finite State Machine (FSM) based logic circuit.

PART-B: VLSI Lab (Back-end Environment)

• The students are required to design and implement the Layout of the following experiments of any FOUR using CMOS 130nm Technology with Mentor Graphics Tool.

List of Experiments:

1. Inverter Characteristics.
2. Full Adder.
3. RS-Latch, D-Latch and Clock Divider.
4. Synchronous Counter and Asynchronous Counter.
5. Static and Dynamic RAM.
6. ROM
7. Digital-to-Analog-Converter.
8. Analog-to-Digital Converter.

Lab Requirements:

Software:

Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL, Mentor Graphics Back End/Tanner Software tool.

Hardware:

Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

G. A. Lakshmi

M. Gopala Krishna

Asso. Prof. (K. Thirupathi Rao)

Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18411L11	Digital system design using Verilog and VHDL	0	0	4	2	2

Note: The students are required to design and draw the internal logical structure of the following Digital Integrated Circuits and to develop VHDL and Verilog HDL Source code, perform simulation using relevant simulator and analyze the obtained simulation results using necessary synthesizer. All the experiments are required to verify and implement the logical operations on the latest FPGA Hardware in the Laboratory.

List of Experiments :(Minimum of Ten Experiments has to be performed using FPGA Trainer kit)

1. Realization of Logic Gates
2. Design of Full Adder using 3 modeling systems
3. 3 to 8 Decoder
4. 8 to 3 Encoder (with and without parity)
5. 8 x 1 Multiplexer-and 2x 4 De-multiplexer-
6. 4- Bit comparator
7. D Flip-Flop
8. Decade counter
9. Shift registers
10. 8-bit serial in-parallel out and parallel in-serial out
11. Fast In & Fast Out (FIFO)
12. MAC (Multiplier & Accumulator)
13. ALU Design.

Equipment/Software required:

1. Xilinx software / Equivalent Industry Standard Software
2. FPGA Training Boards
3. Personal computer system with necessary software to run the programs and Implement

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MIC College of Technology

(Autonomous)

I-Year II Semester

Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18412T01	**Embedded System Design**	3	0	0	3	3

UNIT-I

Introducing Microcontroller Family Introduction, The external interface of the Standard 8051, Reset requirements, Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption and Reading Switches.

UNIT-II

ARM Architecture ARM Design Philosophy, Registers, PSR, Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT-III

ARM Programming Model-I Instruction Set: Data Processing Instructions, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT-IV

ARM Programming Model-II Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single- Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions.

UNIT-V

ARM Programming Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

Memory Management Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Content Switch.

TEXT BOOKS:

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

M. Gopala Krishna

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Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18412T02	Low Power VLSI Design	3	0	0	3	3

UNIT-I

Basics of MOS circuits: MOS Transistor structure and device modeling MOS Inverters MOS Combinational Circuits - Different Logic Families Sources of Power dissipation: Dynamic Power Dissipation Short Circuit Power Switching

UNIT-II

Fundamentals of Low Power VLSI Design Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT-III

Low-Power Design Approaches Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT-IV

Low-Voltage Low-Power Adders Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low- Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT-V

Low-Voltage Low-Power Multipliers Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

Low-Voltage Low-Power Memories Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
2. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
3. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.

M. Gopala Krishna

Anuradha (K. Thirupathi Rao)

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Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18412T03	**Programme Elective- III** **VLSI Signal Processing**	3	0	0	3	3

UNIT-I

Introduction to DSP Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT-II

Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems **Unfolding:** Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT-III

Systolic Architecture Design

Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT-IV

Fast Convolution Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT-V

Low Power Design Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches **Programmable DSP:** Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing.

Numerical strength reduction and PIPELINING: Sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TEXT BOOKS:

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.

2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCE BOOKS:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, 1994, Prentice Hall.

2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

M. Gopala Krishna

(K. Thirupathi Rao)

Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18412T04	**Programme Elective- III** **CMOS Mixed Signal Circuit Design**	3	0	0	3	3

UNIT-I

MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER: MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters.

UNIT-II

Switched Capacitor Circuits Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT-III

Phased Lock Loop (PLL) Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT-IV

Data Converter Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT-V

Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time interleaved converters.

Oversampling Converters Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

M. Gopala Krishna

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MIC College of Technology

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Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18412T05	Programme Elective- IV CPLD and FPGA Architectures and Applications.	3	0	0	3	3

UNIT-I

Introduction to Programmable Logic Devices Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/ Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II

SYSTEM LEVEL DESIGN: Controller, data path and functional partitions, Parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

UNIT-III

Field Programmable Gate Arrays Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT –IV

SRAM Programmable FPGAs Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT –V

Anti-Fuse Programmed FPGAs Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

Design Applications General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/ Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

M. Gopala Krishna

(K. Thirupathi Rao)

Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18412T06	**Programme Elective- IV** **Micro Electro Mechanical Systems (MEMS) Design**	3	0	0	3	3

UNIT-I

Introduction: Basic structures of MEM devices – (Canti-Levers, Fixed Beams diaphragms). Broad Response of Micro electromechanical systems (MEMS) to Mechanical (Force, pressure etc.) Thermal, Electrical, optical and magnetic stimuli, compatibility of MEMS from the point of power dissipation, leakage etc.

UNIT-II

Mechanical concepts: stress, strain, bending moment, deflection curve. Differential equations describing the deflection under concentrated force, Distributed force, distributed force, Deflection curves for canti-levers- fixed beam.

UNIT-III

Electrostatic excitation: columbic force between the fixed and moving electrodes. Deflection with voltage in C.L, Deflection Vs Voltage curve, critical fringe field – field calculations using Laplace equation. Discussion on the approximate solutions – Transient response of the MEMS.

UNIT-IV

Types: Two terminal MEMS - capacitance Vs voltage Curve – Variable capacitor. Applications of variable capacitors. Two terminal MEM structures. Three terminal MEM structures – Controlled variable capacitors – MEM as a switch and possible applications.

UNIT-V

MEM Circuits & Structures: MEM circuits & structures for simple GATES- AND, OR, NAND, NOR, Exclusive OR, simple MEM configurations for flip-flops triggering applications to counters, converters. Applications for analog circuits like frequency converters, wave shaping. RF Switches for modulation. MEM Transducers for pressure, force temperature. Optical MEMS.

MEM Technologies: Silicon based MEMS- Process flow – Brief account of various processes and layers like fixed layer, moving layers spacers etc., and etching technologies. **Metal Based MEMS:** Thin and thick film technologies for MEMS. Process flow and description of the processes, Status of MEMS in the current electronics scenario.

TEXT BOOKS:

1. MEMS Theory, Design and Technology - GABRIEL. M.Review,R.F.,2003, John wiley & Sons. .
2. Strength of Materials –Thimo Shenko, 2000, CBS publishers &Distributors.
3. MEMS and NEMS, Systems Devices; and Structures - ServeyE.Lyshevski, 2002, CRC Press.

REFERENCE BOOKS:

1. Sensor Technology and Devices - Ristic L. (Ed) , 1994, Artech House,London.

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MIC College of Technology

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Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18412T07	**Programme Elective- III** **DSP Processors and Architecture**	3	0	0	3	3

UNIT-I

Introduction to Digital Signal Processing Introduction, a Digital signal processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

UNIT-II

Computational Accuracy in DSP Implementations Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT-III

Architectures for Programmable DSP Devices Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT-IV

Programmable Digital Signal Processors Commercial Digital signal processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT-V

Analog Devices Family of DSP Devices Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS:

1. Digital Signal Processors, Architecture, Programming and Applications- B. Venkataramani and M. Bhaskar, 2002, TMH.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.

M. Gopala Krishna

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Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18412T08	**Programme Elective- IV** **Semiconductor Memory Design and Testing.**	3	0	0	3	3

UNIT-I

Random Access Memory Technologies SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies,

UNIT-II

Application Specific: SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT-III

Non-volatile Memories Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT-IV

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT-V

Semiconductor Memory Reliability and Radiation Effects General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques

Advanced Memory Technologies and High-density Memory Packing Technologies

Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

TEXT BOOKS:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma-2002, Wiley.
3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice Hall.

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MIC College of Technology

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Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18412L09	Embedded Design lab	0	0	4	4	2

The Students are required to write the programs using C-Language according to the Experiment requirements using RTOS Library Functions and macros ARM-926 developer kits and ARM-Cortex.

• The following experiments are required to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification. The programs developed for the implementation should be at the level of an embedded system design.

• The students are required to perform at least SIX experiments from Part-I and TWO experiments from Part-II.

List of Experiments:

Part-I:

Experiments using ARM-926 with PERFECT RTOS

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER'S algorithm.
7. Synchronize two identical threads using MONITOR.
8. Reader's Writer's Problem for concurrent Tasks.

Part-II

Experiments on ARM-CORTEX processor using any open source RTOS.(Coo-Cox-Software-Platform)

1. Implement the interfacing of display with the ARM- CORTEX processor.
2. Interface ADC and DAC ports with the Input and Output sensitive devices.
3. Simulate the temperature DATA Logger with the SERIAL communication with PC.
4. Implement the developer board as a modem for data communication using serial port communication between two PC's.

Lab Requirements:

Software:

(i) Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library, COO- COX Software Platform, YAGARTO TOOLS, and TFTP SERVER.

(ii) LINUX Environment for the compilation using Eclipse IDE & Java with latest version.

Hardware:

(i) The development kits of ARM-926 Developer Kits and ARM-Cortex Boards.

(ii) Serial Cables, Network Cables and recommended power supply for the board.

M. Gopala Krishna

(K. Thirupathi Rao)

Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18412L10	VLSI System design Lab-II	0	0	4	4	2

SYSTEMS DESIGN LAB

Systems Design experiments

- **The students are required to design the logic to perform the following experiments using necessary Industry standard simulator to verify the logical /functional operation, perform the analysis with appropriate synthesizer and to verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).**
- **Consider the suitable switching function and data to implement the required logic if required.**

List of Experiments:

1. Determination of EPCs using CAMP-I Algorithm.
2. Determination of SPCs using CAMP-I Algorithm.
3. Determination of SCs using CAMP-II Algorithm.
4. PLA minimization algorithm (IISc algorithm)
5. PLA folding algorithm(COMPACT algorithm)
6. ROM design.
7. Control unit and data processor logic design
8. Digital system design using FPGA.
9. Kohavi algorithm.
10. Hamming experiments.
11. Multipliers

12 DSP processing systems (FFT)

Lab Requirements:

Software: Industry standard software with perpetual licence consisting of required simulator, synthesizer, analyzer etc. in an appropriate integrated environment.

Hardware: Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

M. Gopala Krishna

(K. Thirupathi Rao)

Devineni Venkata Ramana & Dr. Hima Sekhar

MIC College of Technology

(Autonomous)

Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18412T11	Intellectual Property Rights And Patents	2	0	0	0	2

UNIT I

Introduction to Intellectual Property Rights (IPR)

Concept of Property - Introduction to IPR – International Instruments and IPR - WIPO - TRIPS – WTO – Laws Relating to IPR - IPR Tool Kit - Protection and Regulation - Copyrights and Neighboring Rights – Industrial Property – Patents - Agencies for IPR Registration – Traditional Knowledge –Emerging Areas of IPR – Layout Designs and Integrated Circuits – Use and Misuse of Intellectual Property Rights.

UNIT II

Copyrights and Neighboring Rights

Introduction to Copyrights – Principles of Copyright Protection – Law Relating to Copyrights - Subject Matters of Copyright – Copyright Ownership – Transfer and Duration – Right to Prepare Derivative Works –Rights of Distribution – Rights of Performers – Copyright Registration – Limitations – Infringement of Copyright – Relief and Remedy – Case Law - Semiconductor Chip Protection Act.

UNIT III

Patents

Introduction to Patents - Laws Relating to Patents in India – Patent Requirements – Product Patent and Process Patent - Patent Search - Patent Registration and Granting of Patent - Exclusive Rights – Limitations – Ownership and Transfer — Revocation of Patent – Patent Appellate Board - Infringement of Patent – Double Patenting —Patent Cooperation Treaty – New developments in Patents – Software Protection and Computer related Innovations.

UNIT IV

Trademarks

Introduction to Trademarks – Laws Relating to Trademarks – Functions of Trademark – Distinction between Trademark and Property Mark – Marks Covered under Trademark Law - Trade Mark Registration – Trade Mark Maintenance – Transfer of rights - Deceptive Similarities - Likelihood of Confusion - Dilution of Ownership –Trademarks Claims and Infringement – Remedies – Passing Off Action.

UNIT V

Trade Secrets

Introduction to Trade Secrets – General Principles - Laws Relating to Trade Secrets - Maintaining Trade Secret –Physical Security – Employee Access Limitation – Employee Confidentiality Agreements – Breach of Contract –Law of Unfair Competition – Trade Secret Litigation – Applying State Law. Cyber Law and Cyber Crime

References:

1. Intellectual Property Rights (Patents & Cyber Law), Dr. A. Srinivas. Oxford University Press, New Delhi.
2. Deborah E.Bouchoux: Intellectual Property, Cengage Learning, New Delhi.
3. PrabhuddhaGanguli: Intellectual Property Rights, Tata Mc-Graw –Hill, New Delhi

Devineni Venkata Ramana & Dr. Hima Sekhar

MIC College of Technology

(Autonomous)

II Year III Semester

Sr. No.	Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
1	18413T01 18413T02 18413T03	**Programme Elective V** 1. Advanced Computer Architecture 2. ASIC Design 3. Design for IOT	3	0	0	3	3
2	18413T04 18413T05 18413T06	**Programme Elective VI** 1. Image and Video Processing 2. Wireless communications and Networks 3. Graph Theory and Optimization Technique	3	0	0	3	3
3	18413P01	Project Work part-1 Project Stage – I is an integral part of the project work. In this, the student shall complete the partial work of the project which will consist of problem statement, literature review, project overview, scheme of implementation (Mathematical Model/SRS/UML/ERD/block diagram/ PERT chart, etc.) and Layout & Design of the Set-up. As a part of the progress report of Project work Stage-I, the candidate shall deliver a presentation on the advancement in Technology pertaining to the selected dissertation topic. The student shall submit the duly certified progress report of Project work Stage-I in standard format for satisfactory completion of the work duly signed by the concerned guide and Head of the Department/Institute	0	0	20	20	10
Total Credits							16

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MIC College of Technology

(Autonomous)

Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18413T01	**Advanced Computer Architecture**	3	0	0	3	3

UNIT -I: Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, Measuring and reporting performance, Quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, Classifying instruction set- Memory addressing- type and size of operands, Operations in the instruction set.

UNIT –II: Pipelines: Introduction, Basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, Review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT -III: Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

UNIT-IV : ILP Software Approach Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT –V: Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

TEXT BOOKS

1. John L. Hennessy, David A. Patterson – Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier.

REFERENCES

1. John P. Shen and Miikko H. Lipasti – Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing – Kai Hwang, Faye A.Brigs., MC Graw Hill.
3. Advanced Computer Architecture – A Design Space Approach – Dezso Sima, Terence Fountain, Peter Kacsuk , Pearson Ed

M. Gopala Krishna

(K. Thirupathi Rao)

Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18413T02	ASIC Design	3	0	0	3	3

UNIT-I Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. CMOS Logic: Datapath Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells. 10 Hrs

UNIT-II ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages. Programmable ASIC Logic Cells: MUX as Boolean function generators, Actel ACT: ACT 1, ACT2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX. 10 Hrs

UNIT-III Programmable ASIC I/O Cells: Xilinx and Altera I/O Block. Low-level design entry: Schematic entry: Hierarchical design, Netlist screener. ASIC Construction: Physical Design, CAD Tools. Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms. 12 Hrs

UNIT-IV Floor planning Goals and objectives: Floor planning tools, Channel definition, I/O and Power planning and Clock planning. Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Physical Design Flow.

UNIT-V Routing: Global Routing: Goals and objectives, Global Routing Methods, Back-annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge and Area-Routing Algorithms. Special Routing, Circuit extraction and DRC. 10 Hrs

Text Books:

1.Michael John Sebastian Smith, "Application - Specific Integrated Circuits" Addison-Wesley Professional, 2005.

2.Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd edition, Addison Wesley/ Pearson education, 2011.

Reference Books:

1.Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations", Springer, 2011, ISBN: 978-1-4614-1119-2.

2.Rakesh Chadha, Bhasker J., "An ASIC Low Power Primer", Springer, ISBN: 978-1-4614-4270-7.

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MIC College of Technology

(Autonomous)

Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18413T03	Design for IOT	3	0	0	3	3

UNIT I – OVERVIEW IoT:-An Architectural Overview– Building an architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations. M2M and IoT Technology Fundamentals- Devices and gateways, Local and wide area networking, Data management, Business processes in IoT, Everything as a Service(XaaS), M2M and IoT Analytics, Knowledge Management

UNIT II – REFERENCE ARCHITECTURE: IoT Architecture-State of the Art – Introduction, State of the art, Reference Model and architecture, IoT reference Model - IoT Reference Architecture Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views. Real-World Design Constraints- Introduction, Technical Design constraints-hardware is popular again, Data representation and visualization, Interaction and remote control.

UNIT III – IOT DATA LINK LAYER & NETWORK LAYER PROTOCOLS:PHY/MAC Layer(3GPP MTC, IEEE 802.11, IEEE 802.15), Wireless HART, Z-Wave, Bluetooth Low Energy, Zigbee Smart Energy, DASH7 - Network Layer-IPv4, IPv6, 6LoWPAN, 6TiSCH,ND, DHCP, ICMP, RPL, CORPL, CARP

UNIT IV – TRANSPORT & SESSION LAYER PROTOCOLS: Transport Layer (TCP, MPTCP, UDP, DCCP, SCTP)-(TLS, DTLS) – Session Layer-HTTP, CoAP, XMPP, AMQP, MQTT

UNIT V – SERVICE LAYER PROTOCOLS & SECURITY: Service Layer -oneM2M, ETSI M2M, OMA, BBF – Security in IoT Protocols – MAC 802.15.4 , 6LoWPAN, RPL, Application Layer

TEXT BOOKS:

1. Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stefan Avesand, StamatisKarnouskos, David Boyle, "From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence", 1 st Edition, Academic Press, 2014.

2. Peter Waher, "Learning Internet of Things", PACKT publishing, BIRMINGHAM – MUMBAI

REFERENCES BOOKS:

1. Bernd Scholz-Reiter, Florian Michahelles, "Architecting the Internet of Things", ISBN 978-3-642-19156-5 e-ISBN 978-3-642-19157-2, Springer

2. Daniel Minoli, "Building the Internet of Things with IPv6 and MIPv6: The Evolving World of M2M Communications", ISBN: 978-1-118- 47347-4, Willy Publications

3. Vijay Madisetti and ArshdeepBahga, "Internet of Things (A Hands-onApproach)", 1 st Edition, VPT, 2014.

Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18413T04	**Image and Video Processing**	3	0	0	3	3

UNIT-I

Fundamentals of Image processing and Image Transforms: Basic steps of Image processing system sampling and quantization of an Image – Basic relationship between pixels Image Transforms: 2 – D Discrete Fourier Transform, Discrete Cosine Transform (DCT), Discrete Wavelet transforms.

UNIT-II

Image Processing Techniques: Image Enhancement: Spatial Domain methods: Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial filters, Sharpening Spatial filters Frequency Domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, selective filtering Image Segmentation: Segmentation concepts, point, line and Edge detection, Thresholding, region based segmentation

UNIT-III:

Image Compression: Image compression fundamentals – coding Redundancy, spatial and temporal redundancy. Compression models: Lossy and Lossless, Huffmann coding, Arithmetic coding, LZW coding, run length coding, Bit Plane coding, transform coding, predictive coding , wavelet coding, JPEG standards

UNIT-IV

Basic Steps of Video Processing: Analog video, Digital Video, Time varying Image Formation models : 3D motion models, Geometric Image formation , Photometric Image formation, sampling of video signals, filtering operations

UNIT-V

2-D Motion Estimation: Optical flow, general methodologies, pixel based motion estimation, Block matching algorithm, Mesh based motion Estimation, global Motion Estimation, Region based motion estimation, multi resolution motion estimation. Waveform based coding, Block based transform coding, predictive coding, Application of motion estimation in video coding.

TEXT BOOKS:

1. Gonzaleze and Woods ,"Digital Image Processing ", 3rd edition , Pearson education publications.
2. Yao wang, Joem Ostarmann and Ya – quin Zhang, "Video processing and communication ",1st ed , PHI

REFERENCE TEXT BOOK:

1. M. Tekalp ,"Digital video Processing", Prentice Hall International

M. Gopala Krishna

Asso. Prof (K. Thirupathi Rao)

Devineni Venkata Ramana & Dr. Hima Sekhar

MIC College of Technology

(Autonomous)

Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18413T05	**Wireless communications and Networks**	3	0	0	3	3

UNIT -I

The Cellular Concept-System Design Fundamentals: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies- Prioritizing Handoffs, Practical Handoff Considerations, Interference and system capacity – Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference , Power Control for Reducing interference, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems- Cell Splitting, Sectoring .

UNIT –II

Mobile Radio Propagation: Large-Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, The Three Basic Propagation Mechanisms, Reflection-Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection (Two-Ray) Model, Diffraction-Fresnel Zone Geometry, Knife-edge Diffraction Model, Multiple knife-edge Diffraction, Scattering, Outdoor Propagation Models

UNIT –III

Mobile Radio Propagation: Small –Scale Fading and Multipath: Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel-Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time.

UNIT -IV

Equalization and Diversity: Introduction, Fundamentals of Equalization, Training A Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Non linear Equalization Decision Feedback Equalization (DFE), Maximum Likelihood Sequence Estimation (MLSE) Equalizer, Algorithms for adaptive equalization-Zero Forcing Algorithm, Least Mean Square Algorithm, Recursive least squares algorithm.

UNIT -V

Wireless Networks: Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11,IEEE 802.11 Medium Access Control, Comparision of IEEE 802.11 a, b, g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, Hiper Lan, WLL

TEXT BOOKS:

1. Theodore, S. Rappaport, "Wireless Communications, Principle, Practice ", 2nd Ed, 2002, PHI.
2. Andrea Goldsmith, "Wireless Communications", 2005 Cambridge University Press.
3. Kaveh Pah Laven and P. Krishna Murthy, "Principles of Wireless Networks", 2002, PE
4. Gottapu Sasibhushana Rao, "Mobile Cellular Communication", Pearson Education, 2012.

REFERENCE BOOKS:

1. Kamilo Feher, "Wireless Digital Communications", 1999, PHI.
2. William Stallings, "Wireless Communication and Networking", 2003, PHI.

M. Gopalakrishna

(K. Thirupathi Rao)

Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
18413T06	**Graph Theory Optimization Techniques**	3	0	0	3	3

UNIT-I

Paths and Circuits Graphs: – Data structures for graphs – Subgraphs – Operations on Graphs Connectivity – Networks and the maximum flow – Minimum cut theorem – Trees – Spanning trees – Rooted trees – Matrix representation of graphs.

Unit-II

Graphs & Graph Colorings: Eulerian graphs and Hamiltonian graphs – Standard theorems – Planar graphs – Euler's formula – Five colour theorem – Coloring of graphs – Chromatic number (vertex and edge) properties and examples – Directed graphs

Unit-III

Applications Computer Representation of graphs: – Basic graph algorithms – Minimal spanning tree algorithm – Kruskal and Prim's algorithm – Shortest path algorithms – Dijsktra's algorithm – DFS and BFS algorithms.

Unit-IV

Optimization Techniques: Single variable and multivariable optimization – Lagrangian method – Kuhn-Tucker conditions – Random pattern and Random search methods.

Unit-V

Unconstrained Minimization Methods: Classification – Techniques of unconstrained minimization – Scaling of Design variables – Direct search methods – Random jumping method – Grid search method – Univariate method – Hook and Jeeve's method – Newton – Raphson method – Fibonacci method.

TEXT BOOKS

1. Narsingh Deo, "Graph Théory with Applications to Engineering and Computer Science," PHI.

2. Rao S.S., "Engineering Optimizations: Theory and Practice", New Age International Pvt. Ltd., 3rd Edition, 1998.

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II Year IV Semester

Sr. No.	Course Code	Course Title	L	T	P	Contact Hrs./ Wk.	Credits
1	**18414S01**	Comprehensive Viva Voce	0	0	4	4	2
2	**18414P01**	Project Work Part –II In Project Stage – II, the student shall complete the remaining part of the project which will consist of the fabrication of set up required for the project, work station, conducting experiments and taking results, analysis & validation of results and conclusions. The student shall prepare the duly certified final report of project work in standard format for satisfactory completion of the work duly signed by the concerned guide and head of the Department/Institute	0	0	28	28	14
Total Credits							16

M. Gopala Krishna

Ch. Reddy

(K. Thirupathi Rao)